AIP Applied Physics Letters

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Citation: Appl. Phys. Lett. **99**, 162101 (2011); doi: 10.1063/1.3645597
View online: http://dx.doi.org/10.1063/1.3645597
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v99/i16
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Effect of interface states on the instability under temperature stress in amorphous SiInZnO thin film transistor

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(Received 5 July 2011; accepted 13 September 2011; published online 17 October 2011)

The instability of amorphous SiInZnO thin-film transistor with different active layer thickness under temperature stress has been investigated using the density of states extracted directly from capacitance-voltage characteristics. Interestingly, it is found that the instability under temperature stress is inversely proportional to the magnitude of interfacial trap density not the total trap density. This was observed from the decrease of the falling rate of activation energy as increasing interfacial trap density. Therefore, the interfacial trap plays a very important role as a key origin for the negative threshold voltage shift under temperature stress in SiInZnO thin-film transistors. © *2011 American Institute of Physics*. [doi:10.1063/1.3645597]

There has been growing interest in ZnO-based amorphous oxide semiconductors (AOSs), recently, due to their potential application to thin-film transistors (TFTs) of electronic products such as active matrix organic light emitting diode (AMOLED) and active matrix liquid crystal display (AMLCD). The TFTs using ZnO-based AOSs fabricated at low process temperature have shown higher field effect mobility (μ_{FE}) than that of the conventional TFTs using hydrogenated amorphous silicon (Si) active layer (AL).[1–3] Also, the AOS-TFTs have many good advantages, such as high transparency at visible light, abundance in nature, the thermal stability, and the chemical stability.[4,5] Especially, the TFTs with amorphous GaInZnO (GIZO) as a AL have exhibited the μ_{FE} beyond ~10 cm^2/Vs and good stability under various stresses, such as positive/negative bias, illumination, and temperature stress (TS).[6,7] However, the process temperature over 300 °C has been required to fabricate the GIZO-TFTs, showing the degradation of the electrical performances in the case of GIZO-TFTs prepared below 300 °C. Recently, Si doped InZnO (SIZO) TFTs with the high μ_{FE} of ~21.6 cm^2/Vs and comparable stability with that of GIZO-TFTs have been fabricated at the very low process temperature of 150 °C.[8] Accordingly, an amorphous SIZO-TFT can be one of the superior candidates that can replace the conventional Si-TFTs. However, to date, the extensive and systematic investigations related to stability of SIZO-TFTs have not been carried out. The study should be necessarily performed to comprehend and improve the performances of SIZO-TFTs. Density of states (DOSs) of SIZO-TFTs were extracted from multi-frequency method (MFM) (Ref. 9) to investigate in detail the relationship between TS induced instability and trap states in SIZO-TFTs, even though carrier concentration[10] and total trap density[11] can be estimated from the analysis of transfer characteristics.

In this paper, the instability of amorphous SIZO-TFTs with different AL thickness under TS has been investigated through the subgap DOSs extracted from MFM technique using capacitance-voltage (*C-V*) characteristics. The instability under TS was roughly inversely proportional to the interfacial trap density (N_{it}) rather than the total trap density (N_T). This was well agreed with the reduction of the falling rate (FR) of activation energy (E_a) as increasing N_{it}. Consequently, the gate insulator (GI)/channel interface trap was considered as a key origin of the instability under TS in SIZO-TFTs.

Mo, as a gate electrode, was deposited on a glass substrate by direct current sputtering method, and then amorphous SIZO ALs with different thickness were prepared by the radio frequency magnetron sputtering method at room temperature on 200 nm thick SiN_x as a GI. Amorphous SIZO ALs and source/drain (S/D) electrodes were defined by the conventional photolithography and wet etching process. Ti/Au (10 nm/50 nm) as source/drain electrodes was prepared by electron beam evaporation and thermal evaporation methods, respectively. The well defined channel length and width of the SIZO-TFTs were 200 μm and 100 μm, respectively. All of SIZO-TFTs were annealed at 150 °C for 1 h in thermal furnace with N_2

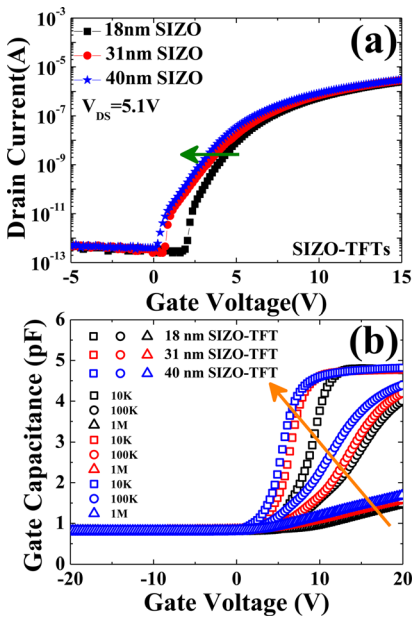

FIG. 1. (Color online) (a) Transfer curves and (b) the frequency dependent *C-V* curves of SIZO-TFTs with different AL thickness.

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TABLE I. Summarization of electrical properties of SIZO-TFTs with AL thickness.

Channel thickness (nm)	V_{th} (V)	μ_{FE} (cm^2/Vs)	$I_{on\text{-}off}$ ratio	SS (V/decade)
18	5.6	16.9	6.5×10^7	0.26
31	4.8	16.9	5.5×10^7	0.39
40	4.1	16.9	5.8×10^7	0.42

ambient. Transfer characteristics were carried out by using semiconductor parameter analyzer (HP 4145B) in dark and vacuum state of $<2 \times 10^{-2}$ Torr. The *C-V* measurements to extract the DOSs in SIZO-TFTs with different AL thickness were performed by using precision LCR meter (Agilent 4284 A).

Figure 1(a) shows the transfer curves of amorphous SIZO-TFTs with different AL thickness. The SIZO AL thickness measured by α-step (AMBIOS, XP-2) was 18, 31, and 40 nm, respectively. Their electrical properties, such as threshold voltage (V_{th}), μ_{FE}, subthreshold swing (SS), and on-off current ratio ($I_{on\text{-}off}$ ratio) were summarized in Table I. The μ_{FE} values at linear region were extracted from transfer curves measured at drain to source voltage (V_{ds}) of 0.1 V, while other parameters were extracted from transfer curves measured at $V_{ds} = 5.1$ V. In particular, the V_{th} of SIZO-TFTs was shifted to negative direction as increasing AL thickness. It can be attributed to the reduction of trap in SIZO-TFT as increasing AL thickness, resulting in the increase of free electron in SIZO AL.[12] Also, the SS values from the SIZO-TFTs were slightly increased with increasing AL thickness, which means the increase of N_{it} in SIZO-TFT. The other parameters such as μ_{FE} and $I_{on\text{-}off}$ ratio showed the similar values in magnitude. The N_{it} of SIZO-TFTs with different AL thickness was estimated by using the following equation:[13]

$$N_{it,\max} = \left[\frac{SS\log(e)}{kT/q} - 1\right]\frac{C_{OX}}{q}, \quad (1)$$

where k is the Boltzmann constant, q is the electron charge, e is the base of natural logarithm, C_{ox} is the capacitance per unit area of GI, and T is the absolute temperature. The N_{it} derived from the SS values was 8.0×10^{11} for 18 nm, 1.1×10^{12} for 31 nm, and $1.2 \times 10^{12}\,cm^{-2}$ for 40 nm thick SIZO-TFT, respectively. Figure 1(b) shows *C-V* characteristics of SIZO-TFTs with different AL thickness. As a result, the measured *C-V* curves are very sensitive to the frequency (f), indicating f dependence on capture-emission events through the interface and/or channel bulk trap.[9] Also, the *C-V* curve was negatively shifted at a given f with increasing AL thickness, meaning the increase of free electron in SIZO-TFT. The *C-V* result is well matched with that of transfer characteristics in terms of the increase of carrier in SIZO-TFT with increasing AL thickness.

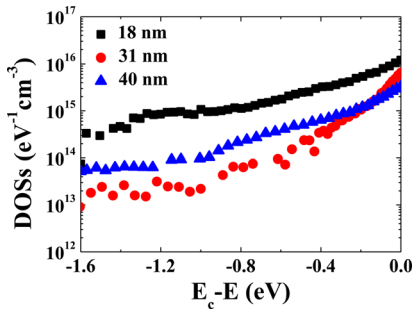

FIG. 2. (Color online) The DOSs of SIZO-TFTs with different AL thickness extracted from MFM technique.

To investigate in detail the distribution and density of tail states and deep states within energy band gap in SIZO-TFTs, the DOSs were extracted from MFM (Ref. 9) method even though N_T can be estimated from analysis of transfer characteristics.[11] Figure 2 shows the subgap DOSs in SIZO-TFTs with different AL thickness. The DOSs only within the energy range from the conduction band (E_c) to ~0.2 eV below E_c were decreased as increasing AL thickness. Based on this result, the further negative V_{th} shift as increasing AL thickness could be also related with acceptor-like (shallow) tail states in SIZO-TFTs. Interestingly, the subgap DOSs in SIZO-TFT was $\sim 10^{16}\,eV^{-1}\,cm^{-3}$ at tail states near E_c, reduced by about ten times compared with that in amorphous GIZO-TFT.[12]

Figure 3 represents the evolutions of V_{th} shift (ΔV_{th}) of SIZO-TFTs with different AL thickness under TS. The V_{th} during TS was shifted to negative direction with increasing

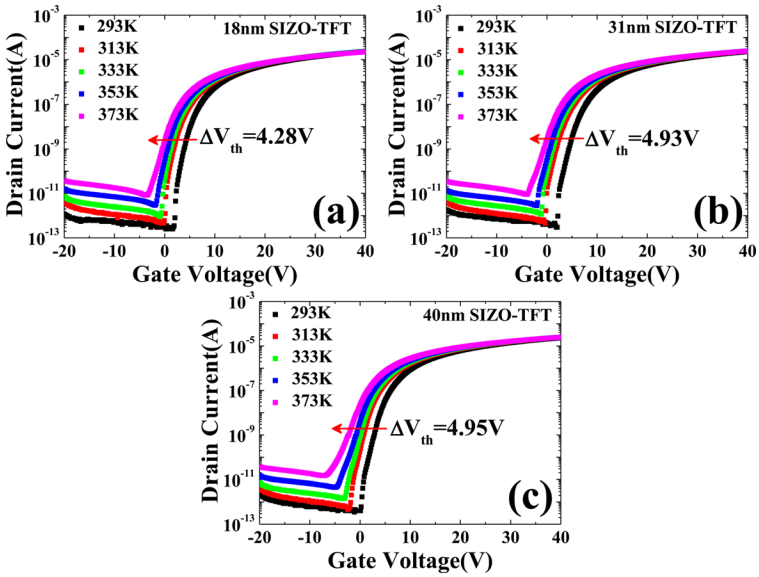

FIG. 3. (Color online) The evolutions of transfer curves of SIZO-TFTs with different AL thickness under TS. (a) ΔV_{th} ~4.28 V for 18 nm thick SIZO-TFT, (b) ΔV_{th} ~4.93 V for 31 nm thick SIZO-TFT, and (c) ΔV_{th} ~4.95 V for 40 nm thick SIZO-TFT, respectively.

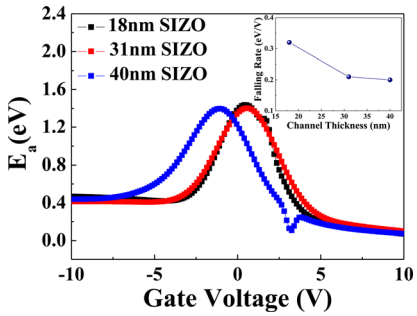

FIG. 4. (Color online) The E_a as a function of V_{gs} of SIZO-TFTs with AL thickness. The inset shows the FRs depending on AL thickness.

temperature. This negative V_{th} shift as increasing temperature can be explained by the thermal activation process of the subthreshold drain current. The subthreshold drain current in ZnO-based AOS-TFTs was well understood by the Arrhenius model,[14–16] where it was assumed that thermally activated electrons from deep trap sites into the E_c moved to the D electrode due to the V_{ds}. The ΔV_{th} under TS was 4.28 V for 18 nm thick SIZO-TFT, 4.93 V for 31 nm SIZO-TFT, and 4.95 V for 40 nm SIZO-TFT. It seems that the ΔV_{th} value under TS is not related to N_T extracted from the subgap DOSs with increasing AL thickness. It is interesting to note that the ΔV_{th} increases as increasing N_{it} in SIZO-TFTs. It was reported that the rate of change in E_F with respect to V_{gs} ($|\Delta E_F/\Delta V_{gs}|$) defined as FR is inversely proportional to the magnitude of N_T in the case of a TFT with a significantly large trap density (N_T) including the DOSs of a semiconductor film and an interfacial trap density of N_{it}. This indicates that the ΔV_{th} under TS increases and FR decreases with increasing N_T.[17,18] To determine the dependence of the FR on N_T or N_{it} in SIZO-TFTs, the logarithm of the $I_{ds}(V_{gs} - V_{th})^{-1}$ versus $(kT)^{-1}$ was plotted using the following equation:[19]

$$I_{ds} \approx \alpha(V_{gs} - V_{th})\exp\left[\frac{-E_a(V_{gs})}{kT}\right], \qquad (2)$$

where I_{ds} is the drain current in subthreshold region, E_a is the activation energy, k is the Boltzmann constant, and α is a constant which does not depend on the temperature and the drain current. Next, the E_a ($= E_c - E_F$) of the subthreshold drain current as a function of gate voltage (V_{gs}) was plotted as shown in Fig. 4. The estimated FR values were 0.32, 0.21, and 0.20 eV $(V)^{-1}$ for 18 nm, 31 nm, and 40 nm SIZO-TFTs,

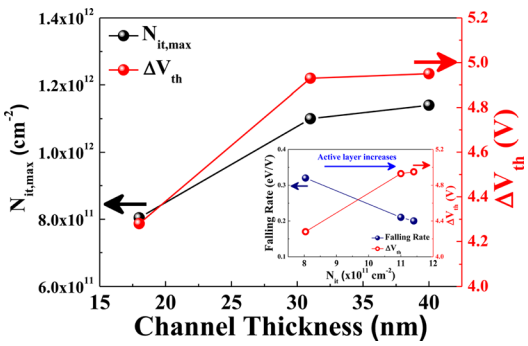

FIG. 5. (Color online) The variation of N_{it} and ΔV_{th} with AL thickness. The inset shows the FRs and ΔV_{th} depending on the N_{it}.

respectively. As increasing AL thickness or N_{it}, the FR value is reduced, showing the clear relationship between FR and N_{it}. However, it is found that there is no correlation between the FR and N_T under our experiment. As a result, the faster FR of 18 nm thick SIZO-TFT, compared to that of other SIZO-TFTs, means that the N_{it} is reduced. The inset in Fig. 4 shows clear relation between the FR and AL thickness.

Figure 5 shows the summarization of our investigation. As increasing AL thickness, the N_{it} and ΔV_{th} increased. Also, the FR value is decreased with increasing N_{it} as shown in the inset in Fig. 5, indicating that the ΔV_{th} under TS increases and FR decreases with increasing N_{it}, not N_T.

In summary, it is found that the stability of amorphous SIZO-TFT under TS was roughly inversely proportional to the magnitude of N_{it}, not N_T or trapping may not play a significant role for the stability of these SiInZnO TFTs. It is also supported by the fact that the FR is closely related with the change of N_{it}. Therefore, it is important to note that detrapping of electrons to E_c at the GI/channel interface traps is a key origin for the ΔV_{th} under TS in SIZO-TFTs.

This work is supported by the IT R&D program of MKE/IITA, Contract No. 82–2–3014–5715 (KI002182, TFT backplane technology for next generation display), as well as the Korea Research Foundation (KRF) grant funded by the Korea government (MEST) (No. 2010-0027759).

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