Optical Charge Pumping Method for Extracting the Energy Level of Interface States in Program/Erase Cycled SONOS Flash Memory Cell and Its Program Time Dependence

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Abstract

Optical charge pumping (CP) technique is proposed as a simple and fast method for extracting the energy distribution of the interface trap D_{it} of silicon-oxide-nitride-oxide-silicon (SONOS) flash memories. It is based on the subthreshold slope change induced by optically excited traps and interface states in SONOS memory cell transistors under sub-bandgap photonic illumination. This technique is advantageous to characterize charge traps in nano-scale emerging devices. The technique has been applied to SONOS CTF memories and investigated the generation and passivation of interface traps as a function of both program/erase cycles and program time.

I. Introduction

Silicon-oxide-nitride-oxide-silicon (SONOS) flash memories have recently attracted much attention as promising next generation EEPROMs. However the degradation of endurance characteristics with a large number of program/erase (P/E) cycles is challenging issue to improve and characterize related mechanisms. In order to investigate degradation mechanisms in the endurance characteristics, it is strongly required to extract the distribution of both interface states in a tunnel oxide/Si substrate (N_{it} [cm^{-3}]) and the bulk traps in the tunnel oxide (N_{OT} [cm^{-3}]) with P/E cycles. Furthermore, the energy distribution of the interface traps (D_{it} [cm^{-2}eV^{-1}]) becomes more important as the thickness of the tunnel oxide decreases, because the charge loss is influenced by the trap-assisted tunneling as well as the thermal emission or Poole-Frenkel emission [1] as schematically shown in Fig. 1.

Up to now, the electrical charge pumping (CP) technique has been widely used for extracting all of N_{OT}, N_{it}, and D_{it} in MOSFETs [2-4]. However, it is very hard to single out the pure charge pumping current (I_{CP}) due to both the electrical pulse setup and the gate leakage current [5, 6]. As an alternative to the electrical CP technique, we have already proposed an optical CP technique as the simple and fast method for extracting D_{it} in SONOS memories [7]. In this work, some critical assumptions in an optical CP technique are reviewed and experimentally verified. Furthermore, its P/E time dependence is investigated.

II. Sub-Bandgap Optical Charge Pumping Model

Under optical illumination with a sub-bandgap photon energy ($E_{ph}<E_{g,Si}$), electrons trapped in the interface traps are excited to Si conduction band E_C without interband electron-hole pair generation in Si substrate as shown in Fig. 2. In order to extract D_{it}, the subthreshold drain current I_D of SONOS memory cell transistor is measured both with and without optical illumination. The detailed procedure of extracting D_{it} from measured I_D in subthreshold bias ($V_{GS}<V_T$) was given in the previous work [7] with related equations and models described by

$$I_D = I_{D0}\exp\left(\frac{V_{GS}-V_{T,dark}}{\eta V_{th}}\right)\left\{1-\exp\left(-\frac{V_{DS}}{V_{th}}\right)\right\}, \quad (1)$$

$$I_{D0} = \mu_{eff} C_{ono}\times\left(\frac{W}{L}\right)\left(\frac{C_d}{C_{ono}}\right)V_{th}^2 = \mu_{eff} C_d\times\left(\frac{W}{L}\right)\times V_{th}^2, \quad (2)$$

$$I_{D,dark} = I_{D0}\times\exp\left[\frac{V_{GS}-V_{T,dark}}{\eta_{dark}V_{th}}\right] \quad for\ V_{DS}>3V_{th}, \quad (3)$$

$$\eta_{dark} = 1+\frac{C_d}{C_{ono}}+\frac{C_{it,dark}}{C_{ono}}, \quad (4)$$

$$I_{D,photo} = I_{D0}\times\exp\left[\frac{V_{GS}-V_{T,photo}}{\eta_{photo}V_{th}}\right] \quad for\ V_D>3V_{th}, \quad (5)$$

$$\eta_{photo} = 1+\frac{C_d}{C_{ono}}+\frac{C_{it,dark}}{C_{ono}}+\frac{C_{it,photo}}{C_{ono}}, \quad (6)$$

$$\frac{1}{\eta_{dark}} \cong \left(\frac{V_{th}}{V_G-V_{T,dark}}\right)\ln\left(\frac{I_{D,dark}}{I_{Do}}\right), \quad (7)$$

$$\frac{1}{\eta_{photo}} \cong \left(\frac{V_{th}}{V_G-V_{T,photo}}\right)\ln\left(\frac{I_{D,photo}}{I_{Do}}\right). \quad (8)$$

Ideality factors (η_{photo} and η_{dark}) can be extracted from the subthreshold slope, and the η_{photo} has a trap-generated additional capacitance $C_{it,\ photo}$ term, and the $C_{it,\ photo}$ is only dependent on the photo-excited carriers in the photo-responsive energy range ($(Ec-E_{ph})<E_t<(E_{Fi}-q\varphi_f+q\varphi_s)$) as shown in Fig. 2. Consequently, optically induced capacitance $C_{it,\ photo}$ can be extracted from the difference between two ideality factors as

$$C_{it,photo} = C_{ono}\times(\eta_{photo}-\eta_{dark}). \quad (9)$$

D_{it}, as a function of V_{GS}, can be consequently obtained from

$$D_{it} = \frac{\Delta C_{it,photo}}{q^2} = \frac{C_{ono}\times(\Delta\eta_{photo}-\Delta\eta_{dark})}{q^2}. \quad (10)$$

Finally, the mapping between the gate bias V_{GS} and the interface trap energy level E_t can be applied to extract the trap density as a function of the trap level. Assuming that the donor-like states exist in the lower half of $E_{g,Si}$ and the acceptor-like states exist in the upper half of $E_{g,Si}$, the value of V_{GS} at a start point of nonzero $\Delta C_{it,photo}$ corresponds to the midgap condition. The range of photo-responsive E_t at the midgap condition is described by

$$E_C - E_{ph}(=1.1-0.95=0.15) < E_t < E_{Fi}(=0.55\ eV)\ @V_{GS}=V_{midgap}.$$

Similarly, when V_{GS} is biased at V_T, the range of photo-responsive E_t is described by

$$E_C - E_{ph}(=1.1-0.95=0.15) < E_t < E_{Fi}+q\phi_f(=0.55+0.356=0.906eV)\ @V_{GS}=V_T.$$

We assume that the change in the surface potential(φ_s) due to sub-bandgap photonic excitation is negligible even though the surface potential is proportional to the gate bias V_{GS}. We also assume that the optical response of electrons trapped in both the nitride storage layer and the border traps in tunnel oxide layer is negligible. As long as these assumptions are valid, two ideality factors can be easily obtained from measured data as shown in Eqs. (7) and (8).

III. Experimental Results and Discussion

I_{DS}-V_{GS} characteristics of the n-channel SONOS memory cell transistors ($W\times L$=0.22μm×0.24μm, O/N/O layer=40/40/40Å) were measured using a semiconductor parameter analyzer combing an optical source with E_{ph}=0.95eV(λ=1310 nm) and the optical power P_{opt}=11.2 mW. Both the P/E scheme-dependence of an optical response and I_{DS}-V_{GS} hysteresis curves are shown in Figs. 4 and 5, respectively. In Fig. 4, the F-N programming is performed with $V_G/V_D/V_S$=13/0/0V, and programming time(T_P) is 10 ms and the CHEI programming was performed with $V_G/V_D/V_S$=5.5/0/5.5V for T_p=5us and the F-N erasing was performed with $V_G/V_D/V_S$=0/13/13 V for T_E=2 ms. The hysteresis in the I_{DS}-V_{GS} curves was independent of the optical illumination as shown in Fig. 5. V_{FB} was extracted by the midgap voltage V_{midgap} and it was not shifted by the optical illumination as shown in Fig. 5. It means that the optical response of charges trapped in the nitride storage layer is negligible because the energy barrier between the nitride and oxide layers (ΔE_C: the discontinuity between conduction bands) is higher than the sub-bandgap photon energy. Furthermore, there is no hysteresis in I_{DS}-V_{GS} curves under optical illumination. It is a strong evidence that the optical response of electrons trapped in the border traps (bulk oxide traps) is negligible under optical illumination. This observation means that assumptions for the constant surface potential under sub-bandgap photonic excitation are valid.

For extracting the evolution of D_{it} with P/E cycles, we used a NAND flash-type scheme (the F-N tunneling-based program and the F-N tunneling-based erase) in the program and erase cycles. The conditions of F-N programming and erasing are the same as those in Fig. 4. In order to investigate the time dependent evolution of D_{it}

and compare the distinction of D_{it}, two different programming times were chosen (T_P=1 ms and 50 ms)keeping the same initial V_T window. Erase time was fixed at T_E=10 ms.

Erased I_{DS}-V_{GS} characteristics under the photonic excitation are comparatively shown in Fig. 6 those under dark condition. As the number of P/E cycles increases, both the subthreshold swing and V_T increase. These results are due to the increased trap electrons excited from interface traps in the photo-responsive energy range to the conduction band and this means increasing D_{it} with P/E cycles.

Fig. 7 shows the extracted D_{it} and its program time dependence. It shows that the energy level of interface trap is higher in the long programming time, but not changed the energy range of interface traps. This is a consequence by increasing of T_P. We also note that interface traps are distributed in the same energy range and shape regardless of the programming time T_P.

IV. Conclusions

Optical CP technique with sub-bandgap photonic excitation is proposed for extracting the interface trap distribution D_{it} in the SONOS charge trap flash memories. Experimental results show that the energy level of interface trap is higher in the long programming time, but not changed the energy range of interface traps. We also found that interface traps are distributed in the same energy range and shapes regardless of the programming time T_P. Proposed optical CP technique is expected to be a reliable method applicable to nano-scale emerging charge trap flash memory devices. There is no electrical pulse during the extraction and the current is measured from not the substrate but the drain contact. It means that a large gate tunneling current can be easily corrected by monitoring both the gate current and drain current, there is no parasitic effect by excluding the pulse measurement setup.

Acknowledgements

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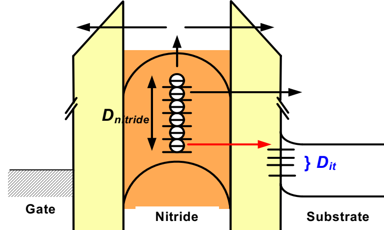

Fig. 1. Charge loss mechanisms in SONOS memory.

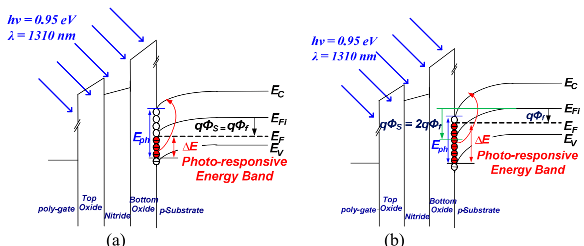

Fig. 2. The energy band diagram of SONOS memory under the optical illumination (E_{ph}<$E_{g,Si}$). The V_G is biased at (a) a midgap-voltage V_{midgap}, and (b) a threshold voltage V_T, respectively.

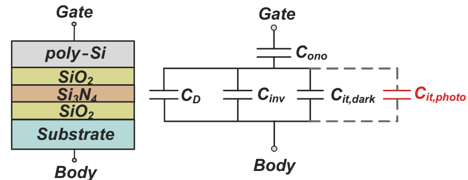

Fig. 3. The equivalent capacitive circuit model for SONOS memory cell transistor.

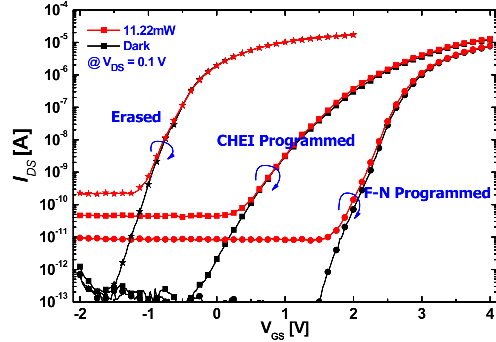

Fig. 4. The Program/Erase scheme-dependence of an optical response

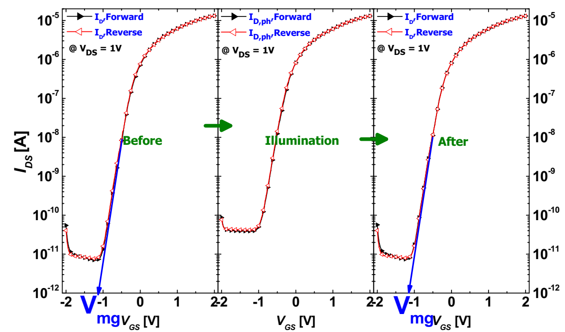

Fig. 5. The I_{DS}-V_{GS} hysteresis curve.

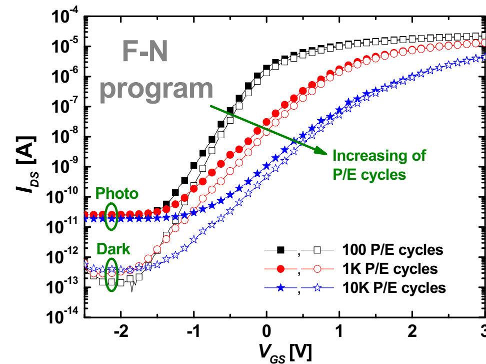

Fig. 6. Erased I_{DS}-V_{GS} characteristics.

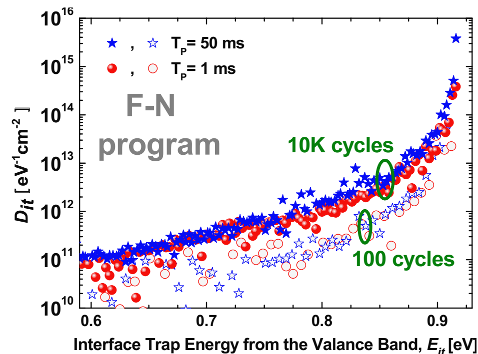

Fig. 7. Extracted D_{it} and its program time dependence