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Analysis of Instability Mechanism under Simultaneous Positive Gate and Drain Bias Stress in Self-Aligned Top-Gate Amorphous Indium-Zinc-Oxide Thin-Film Transistors

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***Abstract*—We quantitatively investigated instability mechanisms under simultaneous positive gate and drain bias stress (SPGDBS) in self-aligned top-gate amorphous indium-zinc-oxide thin-film transistors. After SPGDBS (V_{GS}=13 V and V_{DS}=13 V), the parallel shift of the transfer curve into a negative V_{GS} direction and the increase of on current were observed. In order to quantitatively analyze mechanisms of the SPGDBS-induced negative shift of threshold voltage (ΔV_T), we experimentally extracted the density-of-state, and then analyzed by comparing and combining measurement data and TCAD simulation. As results, 19% and 81% of ΔV_T were taken to the donor-state creation and the hole trapping, respectively. This donor-state seems to be doubly ionized oxygen vacancy (V_O^{2+}). In addition, it was also confirmed that the wider channel width corresponds with more negative ΔV_T. It means that both the donor-state creation and hole trapping can be enhanced due to the increase in self-heating as the width becomes wider. Lastly, all analyzed results were verified by reproducing transfer curves through TCAD simulation.**

***Index Terms*—InZnO, thin-film transistors, positive bias stress, donor-state, hole trapping, self-heating**

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I. INTRODUCTION

Thin-film transistors (TFTs) are the key technology of active-matrix flat-panel displays. Amorphous oxide semiconductor (AOS) TFT technology is a strong candidate because the fabrication process of AOS TFTs is as simple as that of a-Si TFTs even though the performance of AOS TFTs is much superior to that of the a-Si TFTs [1]. Especially, amorphous indium zinc oxide (a-IZO) without Ga should be considered as a promising material, which is suitable for any high frame rate display, such as active-matrix organic light-emitting diodes (AMOLEDs) or system-on-panel applications since it demonstrates higher mobility at high carrier concentration [2, 3].

On the other hand, a-IZO TFT is one of the AOS TFTs, which are still facing with an instability issue under simultaneous positive gate and drain bias stress (SPGDBS) [4]. Also, such instability issues have been analyzed by many research groups and some of them have focused on the negative shift of threshold voltage (ΔV_T) under SPGDBS as well. This degradation effects were electron-hole pairs and self-heating [5]. However, in terms of investigating the degradation mechanism, there have been controversial thoughts: hole trapping into back channel by electron-hole pairs [5, 6], donor-state creation at channel layer [7, 8]. Such mechanisms have not been quantitatively clarified yet including which mechanism is responsible for the ΔV_T.

In this work, a parallel negative shift of the transfer

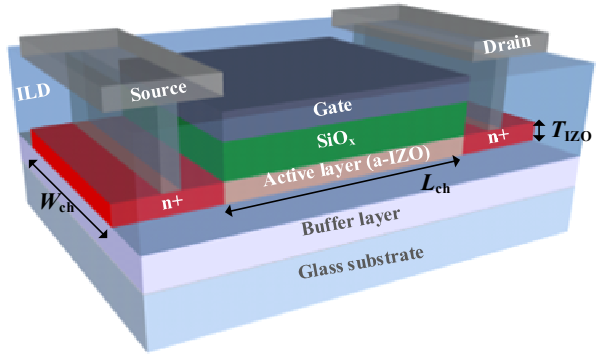

Fig. 1. A schematic view of the self-aligned top-gate a-IZO TFT. Geometrical parameters are W_{ch}=10, 30, 50 μm and L_{ch}=10 μm, T_{IZO}=50 nm

curve under SPGDBS is investigated. The measurement of TFT with various channel widths, temperature and Silvaco Atlas TCAD simulation [9] were employed to verify and quantify the proposed combination mechanism.

II. Device Fabrication and Measurement Results

The self-aligned top-gate a-IZO TFTs used in this study were integrated with a glass substrate as shown in Fig. 1. The fabrication process was as follows. The 50 nm thick a-IZO films (T_{IZO}) were deposited as active layers using radio frequency magnetron sputtering at room temperature (RT). The sputtering gas was composed of Ar and O_2 of 100:1 flow rate. Also, the sputtering target which was used for the a-IZO deposition has 1:1 In:Zn atomic ratio, and the active layers were patterned by wet etching. After that, the N_2O plasma treatment was implemented for 120 s on the active layer pattern. Subsequently, a 100 nm thick SiO_x gate insulator was deposited without vacuum breaking. SiO_x gate insulator was deposited using plasma enhanced chemical vapor deposition (PECVD) at 150°C. Then, 100 nm thick molybdenum (Mo) gate metal was sputter-deposited at RT on the gate insulator. The Mo gate and the SiO_x gate insulator were then patterned by continuous dry etching. After the patterning of the gate and SiO_x gate insulator, the source/drain contact region was treated by Ar plasma for 60 s. After that, 150 nm thick SiO_x interlayer dielectric (ILD) was deposited by PECVD at 150°C and patterned by dry etching. Finally, 200 nm

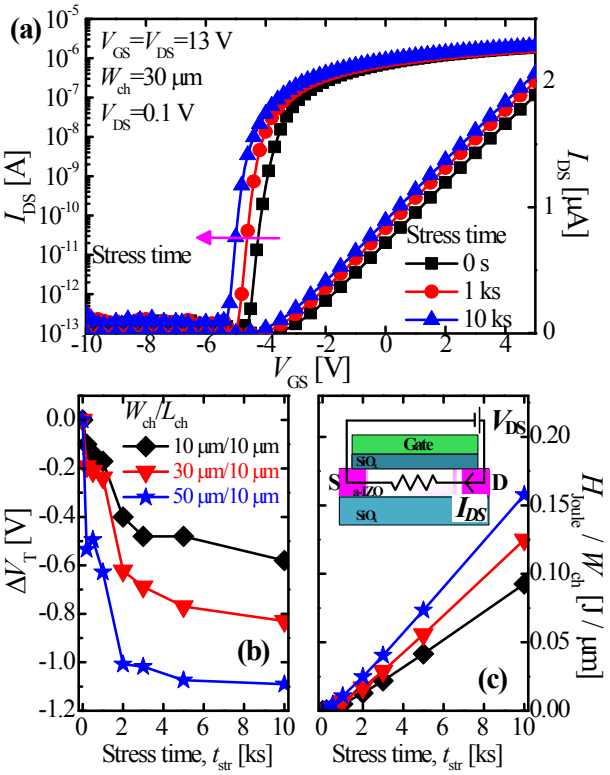

Fig. 2. (a) Transfer curves for SPGDBS, (b) ΔV_T extracted from $I_{CCM}=W_{ch}/L_{ch}$ x 10^{-9} A at various W_{ch} (10, 30, 50 μm) during SPGDBS, (c) Normalized H_{Joule} by W_{ch} during SPGDBS. Inset shows the equivalent circuit describing V_{DS} and I_{DS} through a current path

thick Mo source/drain metal was sputtered at RT and patterned by dry etching.

The followings are results of the measurement and Fig. 2(a) represents the measured transfer curves with stress time (t_{str}) through an Agilent 4156C precision semiconductor parameter analyzer. This curves are measured with V_{DS}=0.1 V at t_{str}=0 s, 1 ks, 10 ks, respectively. The measurements are made at a TFT with channel width (W_{ch})/channel length (L_{ch}) dimension of 30 μm/10 μm. The negative parallel V_T shift of transfer curve is observed during SPGDBS ($V_{GS}=V_{DS}$=13 V). Fig. 2(b) elucidates that increase in W_{ch} (10, 30, 50 μm) corresponds with negative V_T shift (ΔV_T=-0.58, -0.83, -1.09 V) after SPGDBS, respectively. The V_T was extracted by the constant current method ($I_{CCM}=W_{ch}/L_{ch}$ x 10^{-9} A). In addition, since SPGDBS was high current stress, self-heating is generated by Joule heating. It can be calculated by using $H_{Joule}=\int I_{DS} \times V_{DS}\, dt$. Fig. 2(c) signifies that the increase in W_{ch} corresponds with the increase in H_{Joule} normalized by W_{ch}. This is an obvious

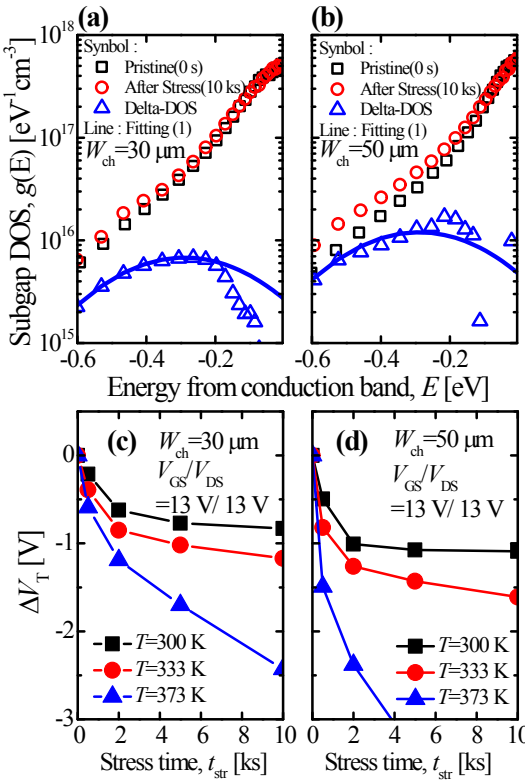

Fig. 3. g(E) of a-IZO was extracted by multi frequency C-V method at (a) W_{ch}=30 μm, (b) W_{ch}=50 μm. The symbols of black square and red circle were the DOS of pristine and after stress, respectively. The blue triangle symbols and blue line are donor-state creation during SPGDBS and fitting curve by Eq. (1). Under SPGDBS, ΔV_T extracted from I_{CCM} at various temperature (300, 333 and 373 K) at (c) W_{ch}=30 μm and at (d) W_{ch}=50 μm

evidence for generation of self-heating because a-IZO has low thermal conductivity and surround with insulator, which is similar SiO_x [10, 11]. Especially, the wider W_{ch} has higher self-heating than narrower W_{ch} during the SPGDBS [6, 8], which is consistent with Fig. 2(c).

III. DISCUSSION

The degradation mechanisms of negative ΔV_T were the hole trapping into back channel by electron-hole pairs and the donor-state creation (*i.e.* oxygen vacancy, zinc interstitial and so on) [12]. While the former is triggered by the impact ionization followed by the generation of electron-hole pairs, the later can be enhanced by collision of hot carrier or self-heating.

In order to analyze the donor-state creation of the active layer, firstly, we extracted subgap density-of-state (DOS) by using multi frequency capacitance-voltage (C-V) method [13] because the collision of hot carrier or self-heating can affect active layer, which performs a current path [7]. Fig. 3(a) and (b) show DOS at pristine (Black square symbol) and after SPGDBS (Red circle symbol), respectively. It was confirmed that the delta-DOS (Blue triangle symbol) is the change amount of DOS during SPGDBS.

$$g_{GD}(E) = N_{GD} \times \exp\left(-\left((E_C + E_0)/kT_{GD}\right)^2\right) \qquad (1)$$

We extracted parameters by fitting through Gaussian Eq. (1). The parameters at W_{ch}=30 μm were N_{GD}= 6.9x10^{15} cm^{-3}eV^{-1}, kT_{GD}=0.3 eV, E_0=0.3 eV and at W_{ch}= 50 μm were N_{GD}=12.1x10^{15} cm^{-3}eV^{-1}, kT_{GD}=0.3 eV, E_0=0.3 eV. The Gaussian donor-state density (N_{GD}) increased at wider W_{ch}. However, Gaussian means energy (E_0) and deviation (kT_{GD}) are the same regardless of variation of W_{ch} shown in Fig. 3(a) and (b). In addition, based on the results shown in Fig. 3(a) and (b), shape of delta-DOS was not only fitted by Eq. (1), energy level of delta-DOS, but also is analogous to the extracted level by other groups [12, 14]. Specifically, it is widely believed that the doubly ionized oxygen vacancy (V_O^{2+}) is observed 0.1~0.3 eV from conduction-band [8, 14]. In addition, V_O^{2+} was extracted by Gaussian function. This oxygen vacancy (V_O) was neutral vacancy because the elimination of an oxygen atom leaves four Zn dangling bonds each contributing 1/2 electron to a neutral vacancy. When electrons come from V_O, it acts as donor-state [15]. Thus, V_O^{2+} should be donor-state, which was observed near the conduction-band edge [12, 14, 15]. Therefore, delta-DOS can be seen as V_O^{2+}. Fig. 3(a) and (b) can be obvious evidences that the increase in W_{ch} correspond with more generating donor-state because the self-heating is increased even more by increase in W_{ch} and the increase in internal temperature of TFT will accelerate V_O^{2+} generation. Also, many groups have studied about the relationship between channel width and temperature [6, 8].

To further verify the heating effect, we conducted experiment shown in Fig. 3(c) and (d). It was observed that ΔV_T is increased according to the increasing temperature at the same W_{ch}, and ΔV_T is increased as W_{ch} increases at the same temperature. We observed that donor-state creation, *i.e.,* generation of V_O^{2+} increases

based on the internal temperature of TFT as shown in Fig. 3(a) and (b); thus, when considering the mechanism of SPGDBS-induced ΔV_T be the donor-state creation, Fig. 3(c) and (d) are well comprehended.

Therefore, to quantitatively analyze the mechanism of SPGDBS-induced ΔV_T, we confirmed whether the donor-state creation shown in Fig. 3(a) and (b) can explain the measurement values of ΔV_T through TCAD simulation. As a result, the donor-state creation can explain only 19% of ΔV_T after the stress as shown in the case (i) in Fig. 5(b). Thus, ΔV_T cannot quantitatively be explained only through donor creation caused by V_O^{2+}.

So, we additionally study the other mechanism, which is hole trapping. To verify the possibility of hole trapping, we use Silvaco Atlas TCAD simulation. The two-dimension (2-D) simulation structure is shown in Fig. 4(a) and specific parts are marked by dashed lines (X_1, X_2, Y). We verified vertical (Y) and lateral near gate insulator (X_1) electric field at SPGDBS shown in Fig. 4(b) and (c), respectively. The electron-hole pair can be generated by impact ionization at drain edge [6, 16] because SPGDBS is high current stress as shown in Fig. 4(b). While electrons got out through the drain, holes would be trapped by high electric field into buffer layer during SPGBDS as shown in Fig. 4(c).

We performed transient simulation to verify the possibility of hole trapping into buffer layer. As the simulation result in Fig. 4(d) indicates, we verify a large amount of hole trapping in buffer during SPGBDS. In addition, we observed that the increase in W_{ch} corresponds with the increase in concentration of trapped hole. However, the impact ionization rate was ~10^{17} $cm^{-3}s^{-1}$ and unrelated to W_{ch}. But, as shown in Fig. 4(f), the increase in W_{ch} correspond with the increase in lattice temperature ($T_{Lattice}$). Thus, the increase in trapped hole by the increase of W_{ch} can be explained with the increase in probability of trapping generated by W_{ch}, not the hole concentration. This also can be well explained through thermally enhanced hole trapping into buffer layer due to the self-heating [6, 16]. Since thermal emission enhances the hole trapping by Poole-Frenkel effect in simulation [17], wider W_{ch} corresponds with concentration of hole trapping in the buffer layer under SPGDBS simulation shown in Fig. 4(d).

To verify quantitatively the effect of two mechanisms, the measured transfer curves (symbol) are compared with

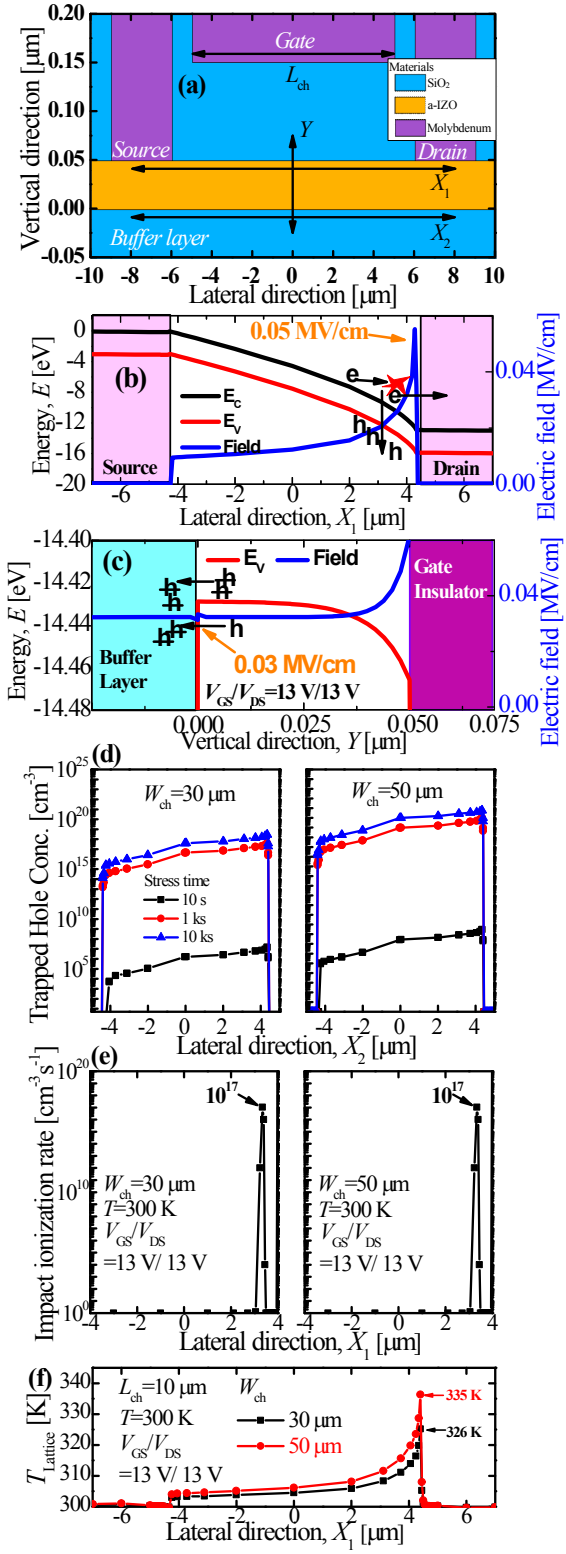

Fig. 4. (a) A schematic view of 2-D top-gate structure at simulation. At SPGDBS condition, (b) energy band diagram and electric field distribution along X_1-direction, (c) vertical Y-direction, respectively, (d) Trapped hole concentration at X_2-direction at t_{str}=10 s, 1 ks, 10 ks with W_{ch}=30, 50 μm, (e) Impact ionization rate, (f) Lattice temperature ($T_{Lattice}$) along X_1-direction

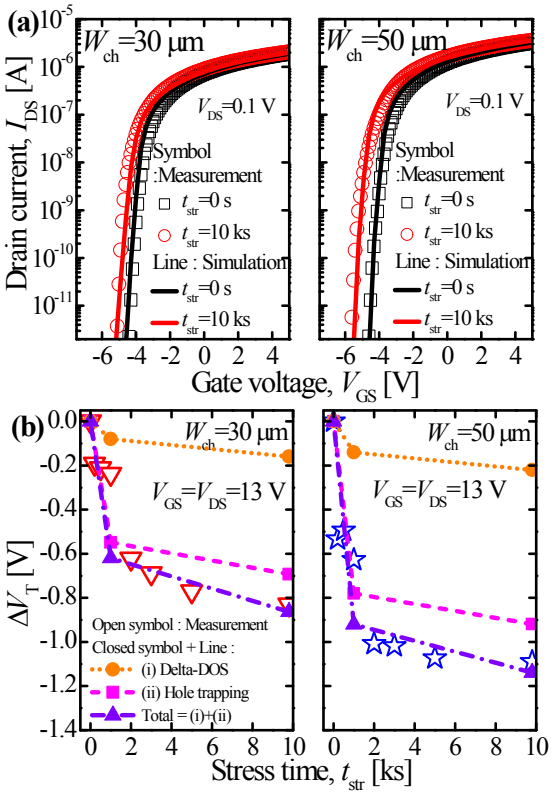

Fig. 5. At W_{ch}=30, 50 μm, measured (a) transfer characteristics of a-IZO TFTs are compared with the atlas simulation curve at 0, 10 ks, (b) ΔV_T by (i) delta-DOS, (ii) hole trapping, (i)+(ii) total (Closed symbol line) and measurement (Open symbol) versus t_{str}

the simulated transfer curves (line) of W_{ch}=30 and 50 μm at t_{str}=0 and 10 ks shown in Fig. 5(a), respectively.

In addition, the extracted ΔV_T along t_{str} at W_{ch}=30 and 50 μm was shown in Fig. 5(b), respectively. As a result, the total ΔV_T reproduces the measured ΔV_T very well. Based upon the simulated and extracted results in our study, it is confirmed that the mechanisms of negative ΔV_T shift were both (i) delta-DOS (19%) (ii) hole trapping (81%) at W_{ch}=30 and 50 μm even though W_{ch} is different. In addition, it is important to take a notice that both (i) delta-DOS and (ii) hole trapping were affected by self-heating, *i.e.*, W_{ch}.

IV. Conclusion

The SPGDBS-induced instability mechanism was quantitatively investigated in self-aligned top-gate a-IZO TFTs. As a result, it is identified that the portion of ΔV_T of donor-state creation takes up 19%, and the 81% of ΔV_T is for the hole trapping. These two mechanisms are enhanced based upon the internal temperature of TFT and thus, it can properly explain the increase in ΔV_T by self-heating due to the increase in W_{ch}. All analyzed results were verified by reproducing transfer curves through TCAD transient simulation. The discussed mechanisms and simulation results are expected to be useful in quantitatively characterizing the instability of high performance oxide TFT at AMOLED operating condition.

Acknowledgments

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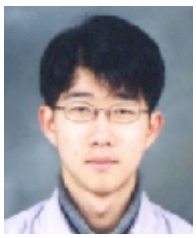

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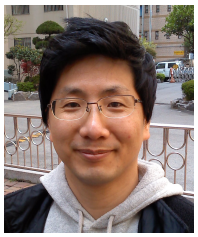

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